

transistors 2351 and 2352 provide the rest current for the ramp. However, if the voltage through 2346 is slow enough, then the voltage input to transistor 2343 will be grounded, and transistor 2343 will not provide current to current mirror to reset capacitor 2337, thus allowing the ramp to continue upward.--

IN THE DRAWINGS

Please amend Figures 3 and 16-22 as shown in red on the attached sheets. An amended drawing in black, with the changes incorporated therein, is also attached.

REMARKS

This preliminary amendment places the application in a better condition for examination. The Applicant(s) respectfully submit that no new matter has been added.

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Respectfully Submitted

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please add the following cross-reference to related application section:

This is a continuation of, and claims the benefit of the filing date of, U.S. Patent Application Serial No. 10/176,712, filed June 20, 2002, entitled Power Converter With Low Loss Switching, which is a continuation of U.S. Patent Application Serial No. 09/778,697 filed February 7, 2001, entitled Power Converter With Low Loss Switching, which is a continuation of U.S. Patent Application Serial No. 09/495969, filed February 2, 2000, entitled Power Converter With Low Loss Switching, which issued July 24, 2001 as Patent No. 6,266,257, which is a divisional of, and claims the benefit of the filing date of, U.S. Patent Application Serial No. 09/111,950, filed July 9, 1998, entitled Power Converter With Low Loss Switching, which issued on September 5, 2000 as U.S. Patent No. 6,115,273.

Paragraph beginning at page 11, line 27, has been amended as follows:

--A pre-regulator 204 receives the rectified sinusoid from rectifier 202 [102] and provides a dc bus output to an output inverter 205. Pre-regulator 204, in the preferred embodiment is a soft-switch boost convertor which provides close to a unity power factor. Other convertor and [pr] inverter configurations may be used. Pre-regulator 204 also allows the input voltage to be anywhere within a range of input voltages in the preferred embodiment.--

Paragraph beginning at page 13, line 23, has been amended as follows:

--Eventually all of the current from inductor L1 flows through switch Z1, and current in inductor L2 drops until it becomes zero, and then reverses. Capacitor C2 discharges through capacitor C1, diode D3, and inductor L2, as shown in Figure 7, by arrow 701. Capacitors C1 and C2 allow diode D1 to turn off with a SVT, thus reducing losses. The discharge occurs at a resonant frequency determined by the time constant of the inductance of inductor L2 and the series capacitance of capacitors C1 and C2 ($f = 1 / (2\pi \sqrt{L2 * (C1 * C2 / (C1 + C2))})$ [1/(2 π $\sqrt{L2 * (C1 + C2 / (C1 * C2))}$)]). The time it takes for capacitor C2 to discharge is the SVT time for diode D1.--

Paragraph beginning at page 17, line 6, has been amended as follows:

--A transistor 1646 limits the output current of op amp 1641, and is controlled by a resistor 1647 (20K ohms) and a diode 1648 [1642]. The input to op amp 1650 is a scaled bus voltage, and sets the maximum output command. The output command (VCOMM) is used to force the current shape to match the input voltage shape.

Paragraph beginning at page 17, line 26, has been amended as follows:

--The command signal is summed with a current feedback signal from a CT1 by an op amp 1670 and provided to [be] a boost drive circuit [1660] through logic gates (not shown) to turn on and off the IGBT in the preregulator. A CT is used to provide current feedback (rather than an LEM for example) because if a LEM fails it will call for unlimited current.--

Paragraph beginning at page 17, line 33, has been amended as follows:

--The boost drive signal is a digital signal of either zero (IGBT ON) or fifteen volts (IGBT OFF). The boost drive input is provided to the base of a pair of transistors [1661] and [1662] because the logic gates output do not provide enough current to drive the IGBT's. Thus, the transistors [1661 and 1662] provide sufficient current. A transistor [1663] level shifts. The gates of a pair of transistors [1665 and 1666] are tied together by a capacitor [1667] (0.1 μ F).--

Paragraph beginning at page 18, line 25, has been amended as follows:

--Capacitor 1512 is switched across transformer 1509 by switches 1502 and 1504. Switches 1402 and 1403 are used to soft switch switches 1502 and 1504. Switches 1402 and 1403 do not need any special timing, and run with the main clock at effectively 50% duty cycle. For example, switches 1502 and 1402 turn on together, and switch 1502 delivers current to transformer 1509, while switch 1402 does nothing. When switch 1502 turns off, switch 1402 remains on, and current is directed through switch 1402 and diode 1405 into capacitor 1512, thus giving an SVT (Slow Voltage Transition) turn off. Switch 1402 is turned off after the transition and diode 1405 prevents the back flow of current from capacitor 1512. This occurs in complimentary fashion with switches 1502 [1501] and 1402 and diode 1405. Thus, this circuit provides full-wave transformer usage, PWM control, complete capacitor balance control with no extra circuitry, and efficient use of switches with SVT.--

Paragraph beginning at page 20, line 29, has been amended as follows:

--Figure 16 shows a control circuit for controlling the switching of the switched snubber in Figures 14 -- 22. Four gate drives 1402A, 1403A, 1502A, and 1504A [1402A -- 1405A] are used to provide the gate signals for switches 1402, 1403, 1502, and 1504, [1402 -- 1405] respectively. These gate drives are not shown in detail and are conventional gate drives such as those found in the Miller XMT 304®. The gate drives are inverting in that a high input [output] maintains the gates off and a low input [output] maintains the gates on [off].--

Paragraph beginning at page 21, line 3, has been amended as follows:

--Gates drivers 1402A, 1403A, 1502A, and 1504A [1402A -
- 1405A] are controlled by a logic circuit 2301. Logic circuit 2301 includes a plurality of NAND and OR gates in the preferred embodiment, however it's specific construction may be any of the designer's choosing. And enable signal is included as an input to logic circuit 2301, in one embodiment. The enable signal is used only during power down.--

Paragraph beginning at page 22, line 10, has been amended as follows:

--A current source including transistors 2336 [2330] and 2331 and resistors 2333 (332 ohms), 2334 (100 ohms) and 2335 (9100 ohms). The current source sets the slope of the ramp. When a capacitor 2337 (100 pF) discharges to a threshold set by a diode 2338 the ramp is restarted. The ramp will continue up at the slope set by the current source until the capacitor voltage reaches the threshold set by op amp 2315 and its circuitry.--

Paragraph beginning at page 23, line 8, has been amended as follows:

--A voltage divider including resistors 2342 and 2345 (68.1K ohms) is tied to a diode 2346. If diode 2346 pulls down the voltage at one end of resistor 2345, then the voltage across a resistor 2347 (5.11K ohms) is also pulled down. A current mirror including resistors 2349 and 2350 (100 ohms) and transistors 2351 and 2352 provide the rest current for the ramp. However, if the voltage through 2346 is slow enough, then the voltage input to transistor 2343 will be grounded, and transistor 2343 will not provide current to current mirror to reset capacitor 2337 [2333] , thus allowing the ramp to continue upward.--

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